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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,669	04/30/2001	Radhika Thekkath	MTEC003/00US	8984

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EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/844,669	Applicant(s) THEKKATH, RADHIKA	
	Examiner Christopher S. McCarthy	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5,6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Torrey et al. U.S. Patent 6,145,123.

As per claim 1, Torrey teaches a tracing control method, comprising of initiating tracing of data during execution of a program that includes a plurality of instructions, said tracing initiation being based on a first trace control command embodied in one or more instructions of said program; and halting said tracing based upon a second trace control command embodied in one or more instructions of said program (column 4, lines 2-7; column 6, lines 56-58).

As per claim 2, Torrey teaches the tracing control method of claim 1, wherein said first trace control command generates a trace enable indication and said second trace control command generates a trace disable indication (column 4, lines 23-27).

As per claim 3, Torrey teaches the tracing control method of claim 2, wherein a trace control indication is embodied in a field of a trace control register that is written to upon execution of a trace control command (column 8, lines 58-63).

As per claim 4, Torey teaches the tracing control method of claim 2, wherein said first trace control command is inserted in an entry point to a section of code, and said second trace control command is inserted in an exit point to said section of code (column 6, lines 56-65).

As per claim 5, Torrey teaches the tracing control method of claim 1, wherein said first trace control command and said second trace control command are included within said program prior to execution of said program (column 3, lines 41-56).

As per claim 6, Torrey teaches a method for tracing a section of program code, comprising of executing a program that includes a plurality of instructions, said plurality of instructions including one or more trace control commands, initiating tracing of data upon entering a section of code in said program, said tracing initiation being based on a first trace control command in said program; and halting said tracing upon leaving a section of code in said program, said halting being based upon a second trace control command in said program (column 4, lines 2-7; column 6, lines 56-65).

As per claim 7, Torrey teaches the method of claim 6, wherein said first trace control command generates a trace enable indication and said second trace control command generates a trace disable indication (column 4, lines 23-27).

As per claim 8, Torrey teaches the tracing control method of claim 7, wherein a trace control indication is embodied in a field of a trace control register that is written to upon execution of a trace control command (column 8, lines 58-63).

As per claim 9, Torrey teaches the tracing control method of claim 6, wherein said first trace control command and said second trace control command are included within said program prior to execution of said program (column 3, lines 41-56).

As per claim 10, Torrey teaches a tracing system, comprising: an embedded processor, said embedded processor including, a processor core for executing instructions (column 5, lines 9-11); and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals and by a software- settable trace control register (column 5, lines 25-27; column 10, lines 29-51).

As per claim 11, Torrey teaches the tracing system of claim 10, wherein said embedded processor further includes a trace capture block that receives trace data from said trace generation logic (column 6, lines 31-47; column 3, lines 43-45).

As per claim 12, Torrey teaches the tracing system of claim 11, wherein said trace capture block sends trace data to an off-chip trace memory (column 6, lines 21-23).

As per claim 13, Torrey teaches the tracing system of claim 11, wherein said hardware input signals are received by said trace generation logic from said trace capture block (column 6, lines 52-54; column 10, lines 29-51).

As per claim 14, Torrey teaches the tracing system of claim 10, wherein said embedded processor further includes a trace memory (column 6, lines 21-23).

As per claim 15, Torrey teaches the tracing system of claim 10, wherein said software-settable trace control register includes a trace select field that indicates whether said trace generation logic operates based on controls provided by said hardware input signals or by said software-settable trace control register (column 10, lines 29-51).

As per claim 16, Torrey teaches the tracing system of claim 10, wherein said software-settable trace control register is set by trace control commands that are embodied in one or more instructions of a program (column 3, lines 60-67).

As per claim 17, Torrey teaches the tracing system of claim 16, wherein said trace control commands are included within said program prior to execution of said program (column 3, lines 41-56).

As per claim 18, Torrey teaches a computer program product comprising of computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions, and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals and by a software-settable trace control register; and a computer-usable medium configured to store the computer-readable program codes (column 5, lines 4-11, 25-27; column 10, lines 29-51).

As per claim 19, Torrey teaches a computer data signal embodied in a transmission medium comprising of computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions, and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals and by a software-settable trace control register (column 5, lines 4-11, 25-27; column 10, lines 29-51).

As per claim 20, Torrey teaches a method for enabling a computer to generate a tracing system, comprising: transmitting computer-readable program code to a computer, said computer-readable program code including: computer-readable program code for causing a computer to describe an embedded processor, said embedded processor including a processor core for executing instructions, and trace generation logic that is operative to generate trace data for said instructions executing in said processor core, said trace generation logic capable of being controlled by hardware input signals and by a software-settable trace control register (column 5, lines 4-11, 25-45; column 10, lines 29-51).

As per claim 21, Torrey teaches the method of claim 20, wherein computer-readable program code is transmitted to said computer over the Internet (column 5, lines 39-44).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (703)305-7599. The examiner can normally be reached on M-F, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703)305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
February 26, 2004

ROBERT BEAUSOLIEL
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